32.4 A Spur Suppression Technique for Phase-Locked Frequency Synthesizers

Tai-Cheng Lee, Wei-Liang Lee

National Taiwan University, Taipei, Taiwan

The design tradeoff in a phase-locked frequency synthesizer between the settling time and the amplitude of the ripple is a critical issue. It limits the performance of the channel switching speed, and the magnitude of the reference spurs at the phase-locked loop (PLL) output. A frequency synthesizer with distributed phase frequency detectors (PFDs) and charge pumps (CPs) was presented in [1] for fast settling. However, the loop parameters have been changed. In this work, a spur suppression technique using distributed PFDs and CPs is used to decrease the magnitude of the reference spurs without changing the loop settling behavior. Furthermore, pulse position modulation (PPM) is used to reduce the accuracy required of the analog circuits.

The reference spurs at the PLL frequency synthesizer output are generated by periodic ripples on the control line of the voltage-controlled oscillator. The magnitude of the spur is proportional to the amplitude of the ripples and inversely proportional to the frequency of the ripples [2]. In conventional phase-locked frequency synthesizers, the amplitude of the ripples on the control line is directly effected by the loop design parameters. The frequency of the ripples on the control line is equivalent to the input reference frequency. These two observations leave very little freedom to design the phase-locked frequency synthesizer.

The PLL architecture used here is shown in Fig. 32.4.1. The distributed PFDs/CPs and two delay lines are used to convert one Up/Dn pulse to N pulses with lower amplitudes in one reference cycle, where N is the number of distributed PFDs/CPs used in the PLL. If the pulses are placed with equal time-spacing in one reference period, the equivalent frequency of the ripples on the control line becomes N times larger. With perfect delay and device matching, by using N PFDs and CPs, the VCO output exhibits no sideband at $\pm\omega_{REF}$, and the offset frequency of the nearest sideband is increased by N times, that is, to $\pm N\omega_{REF}$.

To maintain the same loop settling behavior as conventional integer-N frequency synthesizers, the distributed CP currents are scaled down by N. Figure 32.4.2 shows the settling behaviors on the control line for a conventional PLL and PLLs with two and four PFDs/CPs. With the same phase difference input, the frequency changes in one reference cycle are the same in both the conventional and the new architectures. In other words, the slopes of the approximated ramps are the same in both architectures, and so is the gain of the PFD. The scaling down of the CP currents further decreases the magnitude of the spurs without changing the loop settling behavior. N is chosen as four in this work for Zigbee applications [3].

In order to maintain single-loop operation, delay lines with no delay-locked loops (DLLs) are used in this work. With open-loop operation, delay errors are inevitable. To quantify the effect of the delay errors on the new architecture, the ripples on the control line of a PLL with four distributed PFDs/CPs are simplified as narrow rectangular pulses having a width Δt, a height ΔV', and a period T_{REF}, shown on V_{cont} in Fig. 32.4.1. The timing interval t_d between the four pulses in one period denotes the delay time of each delay stage, and it can be expressed as $(T_{REF}/4)\cdot(1 + \alpha)$, where α is the percentage of delay errors. Comparing the coefficient of the first harmonic of the control voltage with that of a conventional architecture [2], the magnitude differences between the spurs of the new and conventional architectures can be expressed as $20\log_{10}(\frac{1}{2}(\cos\frac{3\pi(1+\alpha)}{4}+\cos\frac{\pi(1+\alpha)}{4}))$ dB.

For example, even with α = -0.2 (-20% delay error), the spur magnitude in the new architecture is still 12dB lower than that in the conventional PLL. The calculation and the simulation results are plotted in Fig. 32.4.3.

In order to suppress the effect of the delay errors even further, pulse-position modulation (PPM) is used. Pulse-position modulation encodes message information in the time delay between pulses in a sequence of signal pulses. The pulses on the control line can be pulse-position modulated by a random binary sequence. Therefore, the time interval between each pulse varies every reference cycle, eliminating the periodic behavior on the control line, and the magnitude of the reference sidebands at the VCO output is decreased. The delay time of each delay stage t_d and the delay time difference between the two paths τ determine the suppression of the reference spurs. The spur magnitudes decrease with increasing τ, and reach the maximum suppression when $t_d + \tau/2 = T_{REF}/N$. Because the probabilities of which path the signal will pass are equal, the expected value of the delay time is $t_d + \tau/2$. When it is equal to the ideal delay time T_{REF}/N, the reference sideband at $\pm\omega_{REF}$ offset will be totally eliminated. Further increasing τ will degrade the magnitude suppression. Randomization techniques can reduce the spur level but somewhat increase the phase noise. Interestingly, this PPM randomization technique shapes the spur power by a sinc function, contributing negligible phase noise around the carrier frequency.

To realize the PPM modulation, the delay paths in the proposed architecture are separated into two paths, one is the fast path, and the other is the slow path. As shown in Fig. 32.4.4, a multiplexer controlled by a random binary code (c_n) is inserted at the output of each delay stage to determine which path the signal will take to the following PFD stage. The random binary codes are generated by a pseudo-random binary sequence (PRBS) generator. In order to provide enough randomization, ten linear feedback shift registers are used to generate the PRBS of length 2^{10}-1.

The frequency synthesizer is designed to operate in a conventional mode and the new mode for comparison. The output of the 4.8GHz VCO is divided by two for I/Q LO generators. Figure 32.4.5 shows the 2.4GHz output spectra during lock for the conventional mode, the mode with distributed PFDs/CPs only, and with PPM randomization. The major reference spur is reduced by -3dB and -10dB, respectively. Figure 32.4.6 summarizes the performance of this integer-N frequency synthesizer. Figure 32.4.7 shows the micrograph of the frequency synthesizer. The chip occupies 0.9×1mm^2, and the active area is 0.35×0.5mm^2. It has been fabricated in a 0.18μm CMOS technology and consumes 18mW from a 1.8V power supply.

Acknowledgment:
This work was funded in part by VIA Technologies and the National Science Council (NSC). The authors would like to thank Chip Implementation Center (CIC) for chip fabrication.

References:
[1] D.-K. Park and S. Mori, "Fast Acquisition Frequency Synthesizer with the Multiple Phase Detectors," *IEEE PACRIM Conf. on Communications*, Computers and Signal Processing, vol. 2, pp. 665-668, May, 1991.
[2] Behzad Razavi, RF Microelectronics, Prentice-Hall, Inc., 1998.
[3] IEEE 802.15.4 Standard.

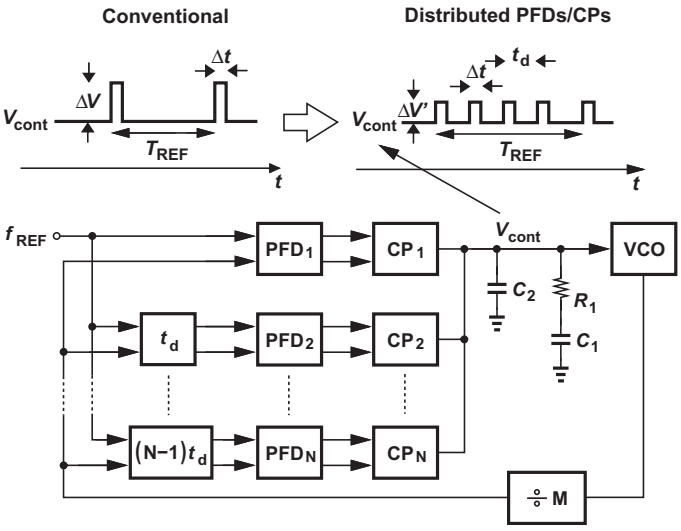

Figure 32.4.1: An integer-*N* frequency synthesizer with distributed PFDs and CPs.

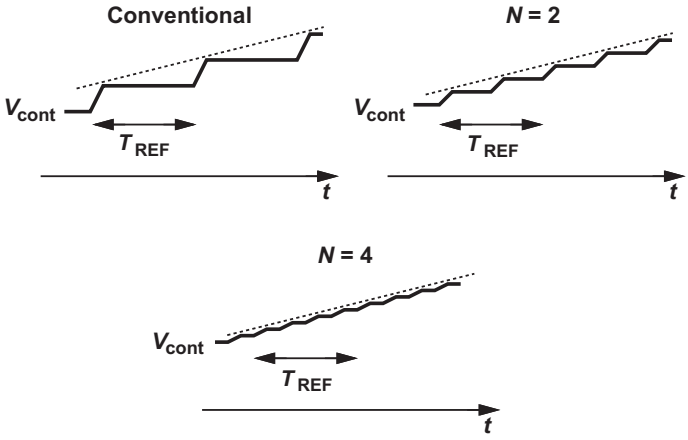

Figure 32.4.2: Settling behaviors of the control line voltage during locking in a conventional PLL and PLLs with two PFDs/CPs and four PFDs/CPs.

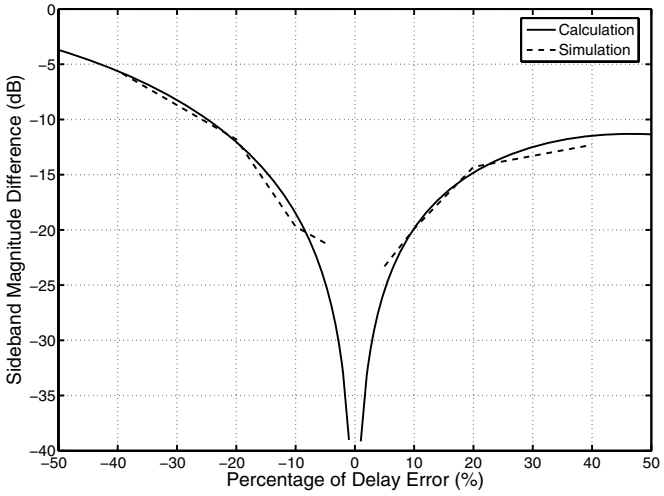

Figure 32.4.3: Percentage of delay error versus the sideband magnitude difference.

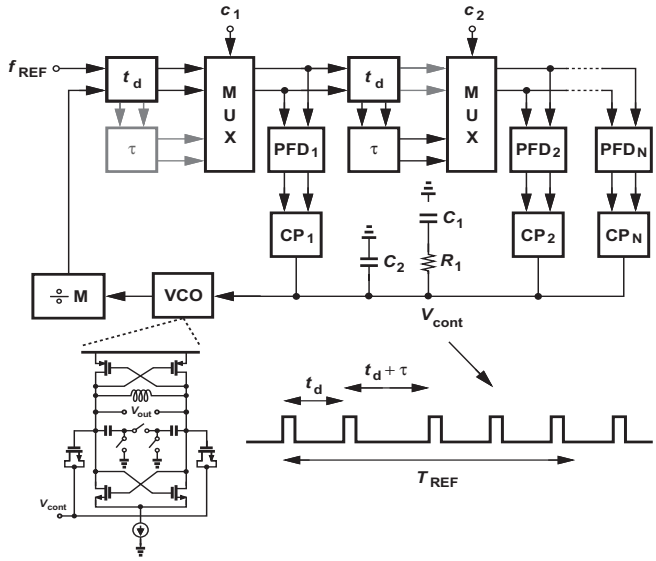

Figure 32.4.4: Frequency synthesizer architecture.

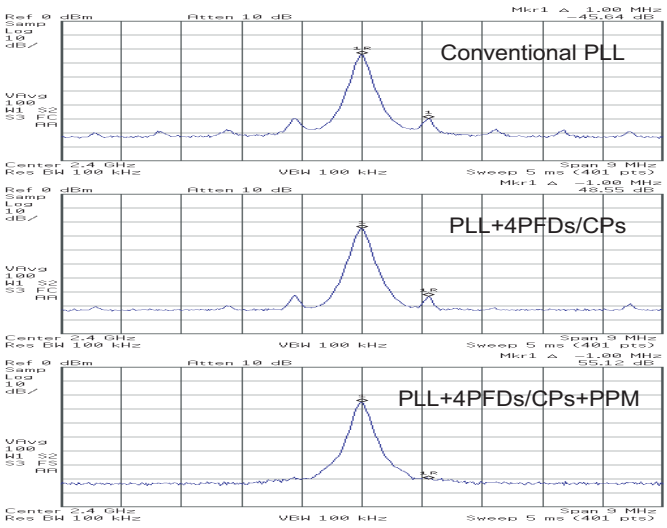

Figure 32.4.5: Measured 2.4-GHz output spectra at lock.

Carrier Frequency	4.8 GHz
I/Q output	2.4 GHz
Reference Frequency	1 MHz
Channel Number	160
Phase noise at 1−MHz offset	
4.8−GHz output	−104 dBC/Hz
2.4−GHz output	−110 dBC/Hz
Spur Level at 1−MHz offset	
Conventional	−45 dBC/Hz
Distributed PFDs/CPs	−48 dBC/Hz
PPM on Vcont	−55 dBC/Hz
Power Dissipation	18 mW
Supply Voltage	1.8V
Die Area	1 mm x 0.9 mm
Technology	0.18−μm CMOS

Figure 32.4.6: Performance summary.

Continued on Page 676

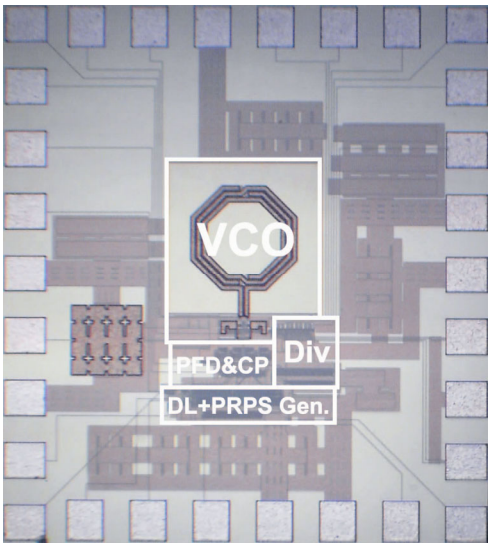

Figure 32.4.7: Chip micrograph.

